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Design and Implementation of Low Leakage SRAM Acrhitectures using CMOS VLSI Circuits in Different Technology Environment

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ABSTRACT: There is a demand for portable devices like mobiles and laptops etc. and their long battery life. For high integrity CMOS VLSI circuit design in deep submicron regime, feature size is reduced according to the improved technology. Reduced feature size devices need low power for their operation. Reduced power supply, reduces the threshold voltage of the device. Low threshold devices have improved performance but sub-threshold leakage current dominates in such a deep submicron regime.Reducing this leakage is a major challenge for CMOS VLSI circuit designers. Many leakage reduction techniques evolved to minimize this leakage. In this paper, we designed a basic one-bit SRAM cell usingsleepy-keeper combined leakage reduction technique in three different technology environments like 120nm, 90nm and 65 nm. Apart from one-bit SRAM cell, we also designed 64-bit SRAM architecture in above three technology environments. We are using Microwind software tool for simulation purpose. We are measuring and comparing the leakage power dissipationin different environments. We observed that improvement in the technology reduces the sub-threshold leakage current and hence leakage power dissipation.

Key-words: Sub-threshold leakage, Deep submicron regime, SRAM Architecture, 120nm, 90nm and 65nm technology environment.

I. INTRODUCTION

Designing of high integrity CMOS VLSI circuits used in almost all portable devices are recommended everywhere. Battery life of such portable devices is to be improved by minimizing the leakage current. To achieve the demand of high integrity ICs, supply voltage should be scaled down. Reduction of supply voltage reduces the threshold voltage of the device. This reduced threshold voltage improves the circuit performance with higher leakage power dissipation. Designing of high integrity circuits with reduced leakage is a challenge for designers.

Memory elements are the critical components in both the high performance processors and portable devices. As a result SRAM consumes most of the power of the system. This becomes a major issue and low power SRAM designs with high performance are in demand in modern VLSI circuit designs. Attention has to be given to reduce the leakage of power in the SRAM cell, in order to improve system power efficiency, performance, reliability and overall costs.

As we move into deep submicron technology, scaling of the transistor threshold voltage sharply increases the sub-threshold leakage current through a transistor when it is off. Low threshold voltage also results in increased sub-threshold leakage current because transistors cannot be turned off completely. For these reasons, static power consumption, i.e., leakage power dissipation, has become a significant portion of total power consumption. There are several CMOS VLSI techniques to reduce this leakage power. Each leakage reduction technique has its own merits and demerits. In this paper, we designed a basic one-bit SRAM cell using sleepy-keeper combined leakage reduction technique in three different technology environments like 120nm, 90nm and 65 nm. Apart from one-bit SRAM cell, we also designed 64-bit SRAM architecture in above three technology environments. We are using Microwind software tool for simulation purpose. We are measuring and comparing the leakage power dissipation in different environments. We observed that improvement in the technology reduces the sub-threshold leakage current and hence leakage power dissipation.

Proposed Work Details

1) Basic one-bit SRAM Cell

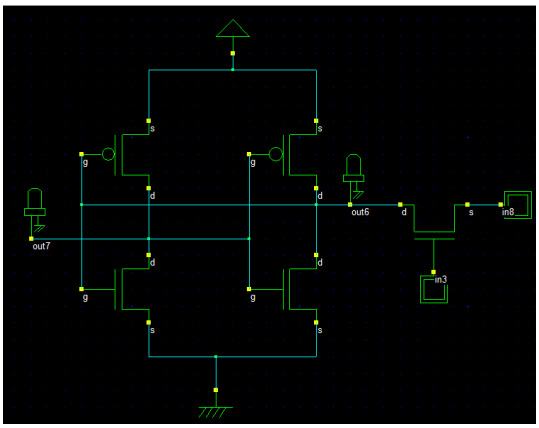

Fig.1. Basic one-bit SRAM Cellusing 120nm,90nm and 65nm.

Fig. 1 is a schematic of Basic one-bit SRAM Cell in which we can store one-bit data either '0' or '1'.

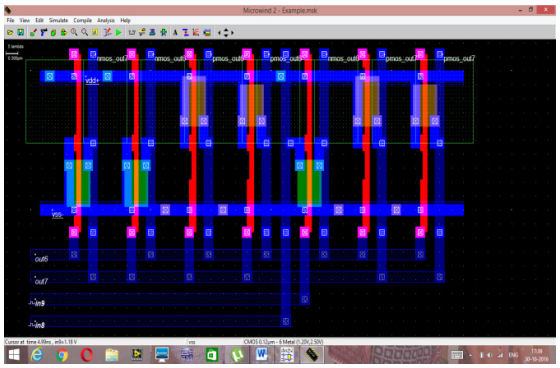

Fig. 2. Layout of Fig. 1

Fig. 2 shows the layout diagram of basic one-bit SRAM Cell

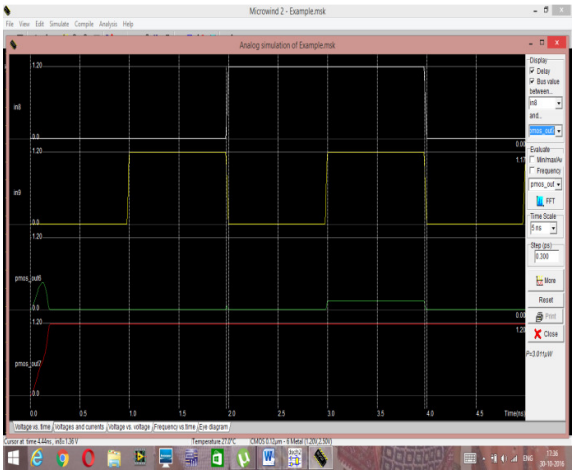

Fig. 3. I/O Timing Diagram of Fig. 2.

Fig. 3 shows the input and output voltage diagrams for the above layout diagram and it also gives the power dissipation of basic one-bit SRAM Cell in 120nm technology Environment.

Fig. 4 shows the basic one-bit SRAM Cell using sleepy with keeper leakage reduction technique in 120nm, 90nm and 65nm technology Environment.

According to forecast Technology parameters, supply voltage V_{DD} for 120nm, 90nm and 65nm technology is taken as 1.2V, 1.0V and 0.9V respectively. Similarly channel length has to be taken as 0.12µm, 0.09µm and 0.065µm for 120nm, 90nm and 65nm respectively in all the cases.

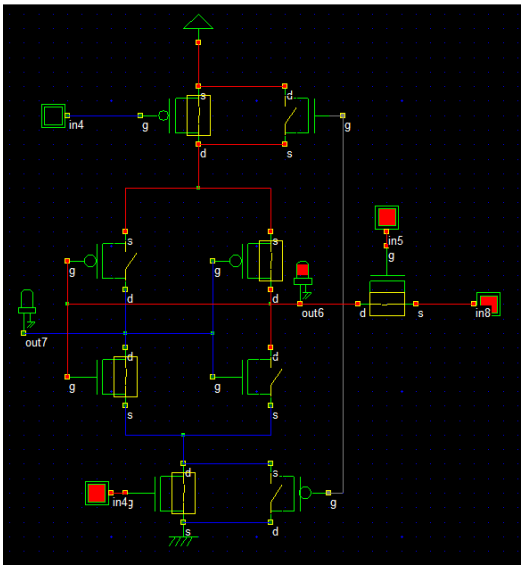

Fig. 4. Basic one-bit SRAM Cell using sleepy-keeper technique in120nm, 90nm and 65nm technology.

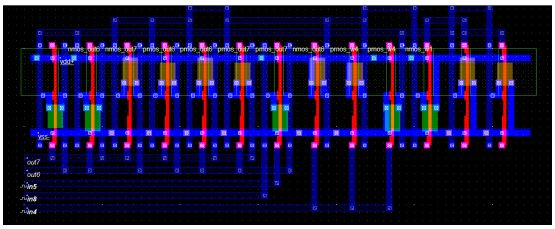

Fig. 5. Layout Diagram of Fig. 5

Fig. 6. Input output Diagram for Fig. 6.

It has 2 pull up PMOS and 2 NMOS pull down transistors as two cross coupled inverters and one NMOS access transistor to access the SRAM cell during Read and Write operations [4]. Both the bit lines (BL and BLB) are used to transfer the data during the read and write operations in a differential manner. To have better noise margin, the data signal and its inverse is provided to BL and BLb respectively. The data is stored as two stable states, at storing points VR and VL, and denoted as 0 and 1.

II. SRAM ARCHITECTURE

A 64-bit SRAM Architectures is shown in Fig. 3. The SRAM array consists of rows and columns of bit cells. For small memory, it is possible to place a word of data in a row; however, in large memories because of space limitation, it is necessary to arrange several words of data in each row. Cells of each column share the same bit-lines. Before the read access, the bit-lines are pre-charged to a known value by the pre-charge circuits (not shown in the figure). The row decoders are used to select a row in the array.

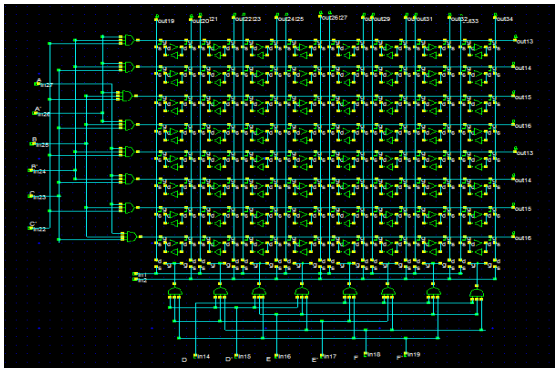

Fig. 7. 64- Bit SRAM Architecture for 120nm,90nm and 65nm Technology.

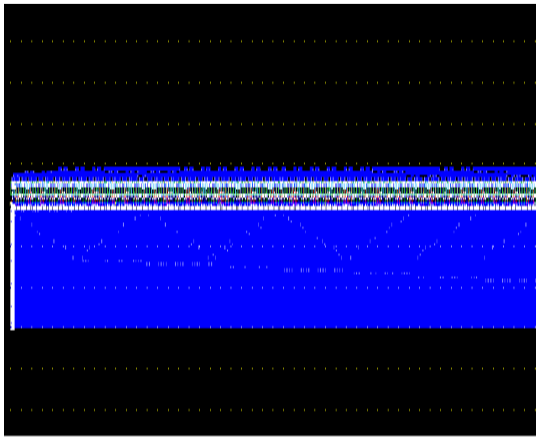

Fig. 8. Layout diagram for 90nm 64- bit SRAM

Depending on the mode of operation, storage cells in the row are connected the common bit-lines and either the stored data in the cell is read by sense amplifiers or overwritten by the write circuits. For larger memories, multiple blocks of the same array are used such that an extra address generator called block address decoder is required.

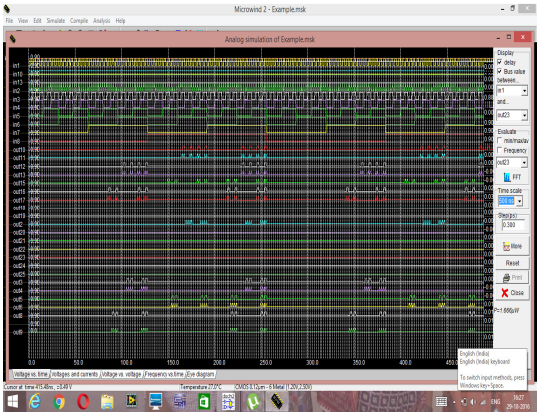

Fig. 9. I/O Timing diagram of 90nm SRAM showing power dissipation.

III. SIMULATION RESULTS

MICROWIND software is used for this approach to analyse the leakage power dissipation at 120nm technology for a power supply (V_{DD}) of 1.2V and channel length (L) will be of 0.12µm, 90nm technology for a power supply ((V_{DD}) of 1.0V and channel length (L) will be of 1.0V and for 65nm technology for a power supply (V_{DD}) of 0.9V and channel length (L) will be of 0.9V.

A SRAM Architectures are simulated at the above said 3-technologies for a given power supply. After analysing the results in terms of static power consumption, we conclude that technology improvement reduces the leakage power dissipation. All schematics are designed and simulated using Microwind EDA tool for a SRAM Cell Array in different approaches using Empirical Level-3 MOS Model and AdvavcedBSIM4 MOS model with 120nm, 90nm and 65nm technologies. Performance characteristic such as static or Leakage power dissipation and Leakage Current is observed using conventional SRAM Cell and 64-bit SRAM Architectures at a temperature of 27 ^{0}C and a Supply voltage, V_{DD} of 1.2V, 1.0V and 0.9V. This static power was measured for 50 ns time interval.

Table 1: Comparison of Leakage Power dissipation and Leakage Currentfor conventional SRAM Cell and SRAM Architectures for 8-bit in 120nm, 90nm and 65nm technologies at V_{DD} is 1.2, 1.0, 0.9 and Channel Length of 0.12µm, 0.09µm and 0.065µm is shown in this table.

Different SRAM Architectures	Technology (nm) and PS-V_{DD}(V)	Static Power dissipation (µw)	Leakage Current (µA)
Basic one-bit SRAM Cell	120; 1.2	4.413	3.677
	90; 1.0	2.100	2.100
	65; 0.9	1.622	1.802
Basic one-bit SRAM Cell with Sleepy-Keeper Technique	120; 1.2	0.965	0.804
	90; 1.0	0.669	0.669
	65; 0.9	0.535	0.594
64-bit SRAM Array	120; 1.2	3.103	2.585
	90; 1.0	2.099	2.099
	65; 0.9	1.381	1.534

CONCLUSION

Performance characteristic such as low leakage power dissipation of a SRAM Architecture is designed and simulated using Microwind software tool in various technologies.In deep submicron regime or in Nano-meter CMOS technology, sub-threshold leakage power is dominant over dynamic power consumption, and thus handling leakage power is a great challenge. In this paper, we proposed a various SRAM Architectures in different environments like 120nm, 90nm and 65nm technologies. It is observed that reduced in technology reduces the leakage power dissipation and Leakage current.In similar manner we design the complex SRAM Arrays in accordance with the demand of memory.Using different leakage reduction techniques, even by using multithreshold devices at different nanotechnologies one can design required apps and get the better performance with minimum leakage power dissipation.

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